Product Introduction

Our SOI (Silicon-On-Insulator) wafers combine a top device silicon layer,buried oxide (BOX) layer, and handle silicon layer, available in diameters from 2" to 8". With tightly controlled thickness tolerances(±5%), low TTV (<5μm) and bow (<20μm), plus flexible doping options(P-type, N-type, intrinsic) and resistivity from 0.001 to over 20,000 Ω·cm, our SOI wafers deliver reliable performance for CMOS,RF, MEMS, and power semiconductor applications.

Applications

- Advanced CMOS logic and low-power ICs
- RF front-end and high-frequency devices
- MEMS sensors and actuators
- Power semiconductor devices requiring dielectric isolation

SILICON ON INSULATOR (SOI) WAFER		
DEVICE LAYER -TOP	MIN.	MAX.
Crystal Growth Method	CZ,FZ	
Diameter	2"	8"
Thickness	0.05μm	> 300μm
Tolerance	±5%	
Crystal Orientation	(100),(110),(111)	
Type/Dopant	P/Boron,N/Phosphorus,Intrinsic	
Resistivity	0.001ohm-cm	> 20000ohm-cm
Front Surface	Polished	
BURIED OXIDE -BOX LAYER	MIN.	MAX.
Thickness	0.1μm	3μm
Tolerance	±5%	
HANDLE LAYER	MIN.	MAX.
Crystal Growth Method	CZ,FZ	
Diameter	2"	8"
Thickness	200μm	750μm
Tolerance	±5%	
Crystal Orientation	(100),(110),(111)	
Type/Dopant	P/Boron,N/Phosphorus,Intrinsic	
Resistivity	0.001ohm-cm	> 20000ohm-cm
Back Surface	Etched or Polished with Oxide	
OVERALL WAFER CHARACTERISTICS	MIN.	MAX.
TTV	< 5μm	
BOW	< 20μm	